

DECLARATION FOR PATENT APPLICATION

01S0984

As a below named inventor, I declare:
that I verily believe myself to be the original, first and sole (if only one individual inventor is listed below) or an original, first and joint inventor (if more than one individual inventor is listed below) of the invention in

FAIL NUMBER DETECTING CIRCUIT OF FLASH MEMORY

the specification of which is attached hereto unless the following box is checked.

was filed on _____ as United States Application
or PCT International Application No. _____, and
was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information of which is material to patentability as defined in 37 CFR 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 35 U.S.C. 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed:

<u>Country</u>	<u>Category</u>	<u>Application No.</u>	<u>Filing Date</u>	<u>Priority Claim</u>
Japan	Patent	2000-335180	November 1, 2000	Yes

And I hereby appoint Donald W. Banner (Reg. No. 17,037), Harold J. Birch (Reg. No. 16,527), Edward F. McKie, Jr. (Reg. No. 17,335), William W. Beckett (Reg. No. 18,262), Dale H. Hoscheit (Reg. No. 19,090), Joseph M. Potenza (Reg. No. 28,175), Alan I. Cantor (Reg. No. 28,163), James A. Niegowski (Reg. No. 28,331), Barry L. Grossman (Reg. No. 30,844), Joseph M. Skerpon (Reg. No. 29,864), Thomas L. Peterson (Reg. No. 30,969), Nina L. Medlock (Reg. No. 29,673), William J. Fisher (Reg. No. 32,133) and Thomas H. Jackson (Reg. No. 29,808), each of whose address is 11th Floor, 1001 G Street, N.W., Washington, D.C. 20001-4597, or any one of them, my attorneys with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent & Trademark Office connected therewith, and request that correspondence be directed to Banner & Witcoff, Ltd., 11th Floor, 1001 G Street, N.W., Washington, D.C. 20001-4597.

I declare further that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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I declare further that my mailing address is at c/o Intellectual Property Division, KABUSHIKI KAISHA TOSHIBA, 1-1 Shibaura 1-chome, Minato-ku, Tokyo 105-8001, Japan; and that my citizenship and residence are as stated below next to my name:

Inventor: (Signature)	Date	Residence
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<u>Ken Takeuchi</u> Ken Takeuchi	<u>Date:</u> OCT. 26.2001	<u>Citizen of:</u> Japan <u>Tokyo, Japan</u>
	<u>Date:</u> _____	<u>Citizen of:</u> Japan _____
	<u>Date:</u> _____	<u>Citizen of:</u> Japan _____